

CLAIMS

WHAT IS CLAIMED:

1. A built-in self-test controller, comprising:
 - 2 a logic built-in self-test engine capable of executing a logic built-in self-test, including:
 - 3 a logic built-in self-test state machine; and
 - 4 a pattern generator seeded with a first primitive polynomial; and
 - 5 a multiple input signature register capable of storing the results of an executed logic built-in self-test, the contents thereof being stored per a second primitive polynomial.
 - 6 2. The built-in self-test controller of claim 1, wherein the first primitive polynomial is $x^{31} + x^3 + 1$.
 - 7 3. The built-in self-test controller of claim 1, wherein the second primitive polynomial is $x^{32} + x^{28} + x + 1$.
 - 8 4. The built-in self-test controller of claim 1, wherein the logic built-in self-test state machine further comprises:
 - 9 a reset state entered upon receipt of an external reset signal;
 - 10 an initiate state entered from the reset state upon receipt of a logic built-in self-test run signal;
 - 11 a scan state entered from the initiate state upon the initialization of components and signals in the logic built-in self-test domain in the initiate state;
 - 12 a step state entered into from the scan state and from which the scan state is entered unless the content of the pattern generator equals a predetermined vector count; and
 - 13 a done state entered into when the content of the pattern generator equals the predetermined vector count.
 - 14 5. The built-in self-test controller of claim 1, wherein the pattern generator comprises a linear feedback shift register seeded with a primitive polynomial.

1 6. The built-in self-test controller of claim 1, wherein the multiple input signature
2 register includes at least one of:

3 a bit indicating whether the logic built-in self-test is done;
4 a bit indicating an error condition arose; and
5 a bit indicating whether the stored results are from a previous logic built-in self-test
6 run.

1 7. The built-in self-test controller of claim 1, wherein the seed for the pattern
2 generator is externally configurable.

1 8. A built-in self-test controller, comprising:
2 means for executing a logic built-in self-test, including a pattern generator seeded
3 with a first primitive polynomial; and
4 means for storing the results of an executed logic built-in self-test, the contents
5 thereof being stored per a second primitive polynomial.

1 9. The built-in self-test controller of claim 8, wherein the first primitive
2 polynomial is $x^{31} + x^3 + 1$.

1 10. The built-in self-test controller of claim 8, wherein the second primitive
2 polynomial is $x^{32} + x^{28} + x + 1$.

1 11. The built-in self-test controller of claim 8, wherein the seed for the pattern
2 generator is externally configurable.

1 12. A integrated circuit device, comprising:
2 a plurality of memory components;
3 a logic core;
4 a testing interface; and
5 a built-in self-test controller, including:
6 a logic built-in self-test engine capable of executing a logic built-in self-test
7 and storing the results thereof, including;
8 a logic built-in self-test state machine; and
9 a pattern generator seeded with a first primitive polynomial; and

10 a multiple input signature register capable of storing the results of an executed
11 logic built-in self-test, the contents thereof being stored per a second
12 primitive polynomial.

1 13. The integrated circuit device of claim 12, wherein the first primitive
2 polynomial is $x^{31} + x^3 + 1$.

1 14. The integrated circuit device of claim 12, wherein the first primitive
2 polynomial is $x^{32} + x^{28} + x + 1$.

1 15. The integrated circuit device of claim 12, wherein the logic built-in self-test
2 state machine further comprises:

3 a reset state entered upon receipt of an external reset signal;
4 an initiate state entered from the reset state upon receipt of a logic built-in self-test run
5 signal;
6 a scan state entered from the initiate state upon the initialization of components and
7 signals in the logic built-in self-test domain in the initiate state;
8 a step state entered into from the scan state and from which the scan state is entered
9 unless the content of the pattern generator equals a predetermined vector
10 count; and
11 a done state entered into when the content of the pattern generator equals the
12 predetermined vector count.

1 16. The integrated circuit device of claim 12, wherein the pattern generator
2 comprises a linear feedback shift register seeded with a primitive polynomial.

1 17. The integrated circuit device of claim 12, wherein the multiple input signature
2 register includes at least one of:

3 a bit indicating whether the logic built-in self-test is done;
4 a bit indicating an error condition arose; and
5 a bit indicating whether the stored results are from a previous logic built-in self-test
6 run.

1 18. The integrated circuit device of claim 12, further comprising:
2 a memory built-in self-test engine; and

3 a memory built-in self-test signature register capable of storing the results of the
4 memory built-in self-test.

1 19. The integrated circuit device of claim 12, wherein the memory components
2 include a static random access memory device.

1 20. The integrated circuit device of claim 12, wherein testing interface comprises
2 a Joint Test Action Group tap controller.

1 21. The integrated circuit device of claim 12, wherein the seed for the pattern
2 generator is externally configurable.

1 22. A method for performing a logic built-in self-test, the method comprising:
2 seeding a pattern generator in a logic built-in self-test engine with a first polynomial;
3 executing a logic built-in self-test using the contents of the pattern generator; and
4 storing the results of an executed logic built-in self-test in a multiple input signature
5 register utilizing a second primitive polynomial.

1 23. The method of claim 22, wherein seeding the pattern generator with the first
2 primitive polynomial includes seeding the pattern generator with the polynomial $x^{31} + x^3 + 1$.

1 24. The method of claim 23, wherein storing the results of the executed logic
2 built-in self-test utilizing the second primitive polynomial utilizes the primitive polynomial is
3 $x^{32} + x^{28} + x + 1$.

1 25. The method of claim 22, wherein storing the results of the executed logic
2 built-in self-test utilizing the second primitive polynomial utilizes the primitive polynomial is
3 $x^{32} + x^{28} + x + 1$.

1 26. The method of claim 22, wherein executing the logic built-in self-test
2 includes:

3 initiating a plurality of components and signals in a logic built-in self-test domain of
4 the dual mode built-in self-test controller upon receipt of a logic built-in self-
5 test run signal;
6 scanning a scan chain upon the initialization of the components and the signals;
7 stepping to a new scan chain; and

8 repeating the previous scanning and stepping until the content of the pattern generator
9 equals a predetermined vector count.

1 27. The method of claim 26, further comprising at least one of:
2 setting a bit in a multiple input signature register indicating whether the logic built-in
3 self-test is done;
4 setting a bit in the multiple input signature register indicating an error condition arose;
5 and
6 setting a bit in the multiple input signature register indicating whether the stored
7 results are from a previous logic built-in self-test run.

1 28. The method of claim 22, further comprising externally configuring the seed.

2 29. A method for testing an integrated circuit device, the method comprising:
3 interfacing the integrated circuit device with a tester;
4 performing a logic built-in self-test, including:
5 seeding a pattern generator in a logic built-in self-test engine with a first
6 polynomial;
7 executing a logic built-in self-test using the contents of the pattern generator;
8 and
9 storing the results of an executed logic built-in self-test in a multiple input
10 signature register utilizing a second primitive polynomial; and
11 reading the stored results.

1 30. The method of claim 29, wherein seeding the pattern generator with the first
2 primitive polynomial includes seeding the pattern generator with the polynomial $x^{31} + x^3 + 1$.

1 31. The method of claim 29, wherein storing the results of the executed logic
2 built-in self-test utilizing the second primitive polynomial utilizes the primitive polynomial is
3 $x^{32} + x^{28} + x + 1$.

1 32. The method of claim 29, further comprising externally configuring the seed.

1 33. The method of claim 29, further comprising performing a memory built-in
2 self-test.